UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,096	07/11/2006	David A. Fish	GB040020	5977

24737 7590 04/13/2010

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
MORRIS, JOHN J	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
04/13/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/597,096	FISH, DAVID A.	
	Examiner	Art Unit	
	John Morris	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-8, 14, 16-17 in the reply filed on 1/19/2010 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 14, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (US Pub# 20030142047 A1).

For **claim 1,** Inoue teaches an active matrix display device comprising an array of display pixels (Inoue, abstract, figure 2), each pixel comprising: a current-driven light emitting display element (Inoue, figure 5, item 56)); a drive transistor (55) for driving a current through the display element (56) (Inoue, figure 5); a storage capacitor (54) for storing a voltage to be used for addressing the drive transistor (55) (Inoue, figure 5); and a light-dependent device (8) for effecting discharge of the storage capacitor in dependence on the light output of the light emitting display element (56) (Inoue, figure 5, paragraphs 72 and 74). Here Inoue teaches the resistance of the light dependent device changing based on the light output from the light emitting display element which affects

the transistors and forms a discharge circuit for the capacitor. Inoue teaches wherein power is provided to each pixel from a first power line (57) (Inoue, figure 5), and wherein one of the light dependent device and the storage capacitor is coupled to a second power supply line (551) (Inoue, figure 5), and wherein the device further comprises means for varying the voltage on the second power supply line (551) during a pixel illumination period (Inoue, figure 6, items C and E, paragraphs 69 and 71).

For **claim 2,** Inoue teaches wherein the voltage on the second power supply line (551) is ramped during a pixel illumination period (Inoue, figure 5 and 6, items 551, C, and E).

For **claim 3,** Inoue teaches wherein the light dependent device (8) comprises a discharge photodiode (Inoue, figure 5, paragraph 69).

For **claim 4,** Inoue teaches wherein each pixel further comprises an address transistor (53) connected between a data signal line and an input to the pixel (Inoue, figure 5).

For **claim 5,** Inoue teaches wherein the drive transistor (55) is connected between a power supply line (57) and the display element (56) (Inoue, figure 5).

For **claim 6,** Inoue teaches wherein each pixel further comprises an isolating transistor (35) connected in series with the drive transistor (Inoue, figure 5).

For **claim 7,** Inoue teaches wherein the storage capacitor (57) is connected between the gate of the drive transistor (55) and one of the first and second power lines (57, 551), and wherein the light dependent device (8) is connected between the gate of the drive transistor (55) and the other of the first and second power lines (57, 551) (Inoue, figure 5).

For **claim 8,** Inoue teaches wherein the storage capacitor (54) is connected between the gate of the drive transistor (55) and the first power line (57), and the light dependent device (8) is connected between the gate of the drive transistor (55) and the second power line (551) (Inoue, figure 5).

For **claim 14,** Inoue teaches wherein each pixel is adapted to draw substantially the same current from the first and second power lines (57, 551) (Inoue, figure 6, paragraphs 69, 72-74).

For **claim 16,** Inoue teaches a method of driving an active matrix display device comprising an array of display pixels (Inoue, figure 2, abstract) each comprising a drive transistor (55) and a current-driven light emitting display element (56) (Inoue, figure 5), the method comprising, for each addressing of the pixel: applying a drive voltage to an

input of the pixel (Inoue, figure 5 and 6, paragraphs 69-77); storing a voltage derived from the drive voltage on a discharge capacitor ((Inoue, figure 5 and 6, paragraphs 69-77); driving the drive transistor (55) using a voltage on a storage capacitor (54) (Inoue, figure 5 and 6, paragraphs 69-77); discharging the storage capacitor (54) using a light sensitive element, at a rate or time dependent on the light output of the display element (56) (Inoue, figure 5 and 6, paragraphs 69-77), and varying a voltage on a terminal of the light sensitive element or the storage capacitor thereby to compensate for leakage currents of the light sensitive element (Inoue, figure 5 and 6, paragraphs 69-77).

For **claim 17**, Inoue teaches wherein a first current is drawn by the drive transistor and a second current is drawn from said terminal of the light sensitive element or the storage capacitor, and wherein the method further comprises matching the first and second currents (Inoue, figure 5 and 6, paragraphs 69-77).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Morris whose telephone number is (571)270-7171. The examiner can normally be reached on Monday-Friday, 7am-3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629